PATENT

## IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant(s): Akhil K. Garlapati et al.

Title: VOLTAGE REFERENCE GENERATOR CIRCUIT USING LOW-BETA

EFFECT OF A CMOS BIPOLAR TRANSISTOR

Application No.: 10/813,837 Filed: March 31, 2004

10/015,05/

Examiner: Patel, Rajnikant B. Group Art Unit: 2838

Atty. Docket No.: 026-0044 Confirmation No.: 6047

January 30, 2006

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Respectfully submitted,

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| PTO/SB/08A (Substitute for form 1449/PTO)     | Attorney Docket No.:  | 026-0044            |
|---|-----------------------|---------------------|
|   | Application No.:      | 10/813,837          |
| INFORMATION DISCLOSURE STATEMENT BY APPLICANT | First Named Inventor: | Akhil K. Garlapati  |
|   | Filing Date:          | March 31, 2004      |
|   | Group Art Unit:       | 2838                |
|   | Examiner Name:        | Patel, Rajnikant B. |
| Sheet 1 of 1                                  | Date Submitted:       | January 30, 2006    |

| Examiner<br>Initials* | Cite<br>No.1             | Document Number<br>Number-Kind Code <sup>2</sup>   | Publication Date<br>MM-DD-YYYY | Name of Patentee or<br>Applicant of Cited Document | Pages, Columns, Lines, Where<br>Relevant Passages or Relevant<br>Figures Appear |   |
|-----------------------|--------------------------|--|--------------------------------|--|---|---|
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| Examiner<br>Initials* | Cite<br>No. <sup>1</sup> | Foreign Patent Document<br>Country Code <sup>3</sup> -Number <sup>4</sup> -<br>Kind Code <sup>5</sup> (if known) | Publication Date<br>MM-DD-YYYY | Name of Patentee or Applicant<br>of Cited Document | Pages, Columns, Lines,<br>Where Relevant Passages or<br>Relevant Figures Appear | T |
|                       | <u>-</u>                 |  |                                |  |   |   |
|                       |                          |  |                                |  | -   |   |
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For Japanese patent documents, the indication of the year of the reign of the Emperor must precede the serial number of the patent document.

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